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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,306	BUSSON ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 10/27/05 in which claims 11-57 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection therefore this case is made final.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ciccarelli et al U.S. patent No 6,498,926 B1 in view of Gilhousen et al Patent No 5,485,486.

As per claim 11, Ciccarelli et al process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected there between, the analog circuit comprising a frequency transposition stage and a first controlled-gain amplifier stage connected upstream (see figs. 2-4) thereof the process comprising: calculating an overall power (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40) of an entire signal having a plurality of channels (see fig.4 element I and Q and col.7, lines 18-28) received by the tuner during a phase initialization; comparing the calculated overall power the digital circuit with a first reference value corresponding to desired power at a predetermined location in the analog circuit (see col.12, lines 39-67 and col.15, lines 1-25); adjusting a

gain of first controlled-gain amplifier; and selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted (see col.8, lines 23-25 and col.17, lines 1-5).

However Ciccarelli et al does not teach adjusting a gain of first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value.

Gilhousen et al teaches adjusting a gain of first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value (see col.16, lines 59-67 and col.17, lines 1-35 and col.18, lines 20-35).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Gilhousen into Ciccarelli as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claim 12, Ciccarelli et al does teach calculating the overall power comprises mean power (see fig.2 element 1290 and col.12, line 13).

As per claim 13, Ciccarelli et al does teach desired power at the predetermined location receiver is a maximum power (see col.12, line 13-67).

As per claims 14, 25, 36 Ciccarelli et al does teach, wherein the gain of the first controlled-gain amplifier stage is adjusted to minimize (see col.12, lines 48-55) the deviation between the calculated overall power and the first reference.

As per claim 15, Ciccarelli et al does teach, wherein the analog circuit further comprises a base band filter (see figs.2 element 1232 and col.7, line 33) connected to

an output the frequency transposition stager (see fig.2 element 1230) and a second controlled-gain amplifier (see fig.2 element 1234) stage connected an output of the base band filter; and the process further comprising: calculating a channel power of the selected channel during the phase of normal operation (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); comparing (see col.12, lines 39-67 and col.15, lines 1-25) the calculated channel power second reference value corresponding a desired channel power desired at an input of the analog/digital conversion stage; adjusting a gain(see col.8, lines 23-25 and col.17, lines 1-5) of the second controlled-gain amplifier stage based.

However Ciccarelli et al does not teach adjusting a gain of second controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value.

Gilhousen et al teaches adjusting a gain of second controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value (see col.16, lines 59-67 and col.17, lines 1-35 and col.18, lines 20-35).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Gilhousen into Ciccarelli as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 16, 23 Ciccarelli et al does teach, wherein comprises calculating a mean power (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40).

As per claims 17, 24, 35 Ciccarelli et al does teach desired power at the predetermined location receiver is a maximum power (see col.12, line 13-67).

As per claims 18, Ciccarelli et al does teach, wherein the gain of the second controlled-gain amplifier stage is adjusted to minimize (see col.12, lines 48-55) the deviation between the calculated overall power and the first reference.

As per claims 19, 31 Ciccarelli et al does teach wherein calculating the overall power of the entire signal is based upon signal available between an output of the first controlled-gain amplifier stage and an input of the frequency transposition stage (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40).

As per claim 20, Ciccarelli et al does teach wherein calculating the overall power of the entire signal is performed in the digital circuit (see fig.2 element 1290).

As per claim 21, Ciccarelli et al does teach, wherein the controlled-gain amplifier stage comprises an attenuator for attenuating the signal (see fig.2 element 1216 and col.7, line 47).

As per claims 22, Ciccarelli et al does teach a process for controlling a tuner having zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected there-between, the analog circuit comprising first controlled-gain amplifier stage and a second controlled-gain amplifier stage with a frequency transposition stage connected there-between the process comprising (see figs. 2-4): calculating an overall power an entire signal having a plurality of channels received by the tuner during phase of initialization(see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); adjusting a gain of the first controlled-gain amplifier

stage (see fig.2 element 1280 and col.6,lines 54-60 and col.7, lines 53-57); selecting one of the plurality channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted (see col.8, lines 23-25 and col.17, lines 1-5); calculating a channel power of the selected channel during the phase of normal operation (see fig.2-3 element 1290 or 1390 and col.12, lines 11-40); and adjusting a gain second controlled-gain amplifier stage a desired channel power at an input of the conversion stage (see figs 2-3 elements 1280,1380 and col.8, lines 23-25 and col.17, lines 1-5).

However Ciccarelli et al does not teach adjusting a gain of first and second controlled-gain amplifier stages based upon a deviation between the calculated overall power and the first and second reference values to a desired power of the analog circuit and digital conversion stage, respectively.

Gilhousen et al teaches adjusting a gain of first and second controlled-gain amplifier stages based upon a deviation between the calculated overall power and the first and second reference values to a desired power of the analog circuit and digital conversion stage, respectively (see figs. 5-6 and col.16, lines 59-67 and col.17, lines 1-35 and col.18, lines 20-35).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Gilhousen into Ciccarelli as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 26, 30, Ciccarelli et al does teach, wherein adjusting the gain the first controlled-gain amplifier stage comprises comparing calculated overall power the first reference value (see col.12, lines 38-67).

As per claims 27, 34, Ciccarelli et al does teach wherein calculating the channel power comprises calculating a mean channel power (see col.12, lines 38-67).

As per claims 28, 32, 35 Ciccarelli et al does teach wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power (see col.12, lines 38-67).

As per claim 29, Ciccarelli et al does teach wherein second controlled-gain amplifier stage is adjusted (see col.12, lines 38-67).

As per claims 33, 46, Ciccarelli et al does teach tuner having a zero intermediate frequency and comprising: an analog circuit comprising a first controlled-gain amplifier (see figs 2-3 element 1220a, 1320a) stage having an input receiving an entire signal having a plurality of channels; a signal routing circuit (see fig.2 element 1224) having an input receiving the entire signal from said controlled-gain amplifier stage, and a frequency transposition stage (see fig.2 element 1230) connected to first output of said signal routing circuit; an analog/digital conversion stage having an input being connected to an output of said frequency transposition stage or to a second output of said signal routing circuit (see fig.4 element 1410); a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired

power at a predetermined location in said analog circuit(see fig.2-3 element 1290 or 1390 and col.12, lines 11-67 and col.15, lines 1-25); and a control circuit connected to said signal routing circuit for connecting the input to the second output thereof (see fig.2 element 1280 and col.6,lines 54-60 and col.7, lines 53-57), and for connecting the input to the first output thereof for selecting (see col.8, lines 23-25 and col.17, lines 1-5) one of the plurality of channels during a phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

However Ciccarelli et al does not teach a control circuit for adjusting a deviation between the calculated overall power and the first reference value during a phase initialization.

Gilhousen et al teaches a control circuit for adjusting a deviation between the calculated overall power and the first reference value during a phase initialization (see figs. 5-6 and col.16, lines 59-67 and col.17, lines 1-35 and col.18, lines 20-35).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Gilhousen into Ciccarelli as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 37, 47, 50 Ciccarelli et al and the Gilhousen's comparator (see figs 5-6 elements 98 or 120) in combination would teach wherein said digital circuit further comprises: first calculator circuit for providing the calculated overall power; and first comparison circuit for comparing the calculated overall power with the first reference value as to provide an output signal indicative of the deviation of the average

power level from the desired power level as taught by Gilhousen (see col.18, lines 25-35).

As per claims 38, 51 Ciccarelli et al and the Gilhousen in combination would teach further base band filter connected to an output of said frequency stage as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 39, 52 Ciccarelli et al teaches wherein said a second controlled-gain amplifier stage (see fig.2 element 1234) connected an output of said frequency transposition stage.

As per claims 40, 49, Ciccarelli et al and the Gilhousen in combination would teach wherein said digital circuit further comprises a second adjustment circuit for adjusting of said second controlled-gain amplifier stage based upon a deviation between a calculated channel power of a selected channel and a second reference value as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 41, 48, 55, 57 Ciccarelli et al and the Gilhousen in combination would teach calculated channel power comprises a mean 40, wherein the channel power as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claim 42, Ciccarelli et al and the Gilhousen in combination would teach wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize

the deviation between the calculated channel power and the second reference value as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claims 43, 53, 56 Ciccarelli et al and Gilhousen's comparator (see figs 5-6 elements 98 or 120) in combination would teach wherein said digital circuit further comprises: a second calculation circuit for providing calculated channel power during a phase of normal operation; and a second comparison circuit comparing the calculated channel power with the second reference value corresponding desired channel power at an input of said analog/digital conversion stage as to provide an output signal indicative of the deviation of the average power level from the desired power level as taught by Gilhousen (see col.18, lines 25-35).

As per claim 44, Ciccarelli et al and the Gilhousen in combination would teach, wherein the desired channel power maximum channel power as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

As per claim 45, Ciccarelli et al and the Gilhousen in combination would teach, further comprising a semiconductor substrate such that said analog circuit, said analog/digital conversion stage, and said digital circuit are integrated on said semiconductor substrate as to compensate for changes in the inbound channel that are independent of the outbound channel as taught by Gilhousen (see col.18, lines 45-55).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kamgar et al U.S Patent no 6,324,387 B1 teaches a LNA control circuit.

MacNally U.S. Patent No 6,516,185 B teaches an AGC control and offset correction.

Ruelke U.S. Patent No 6,459,889 B1 teaches a DC offset correction loop.

Webster et al U.S. Patent No 6,748,200 B1 teaches an AGC control system.

Mohindra U.S. Patent No 6,442,380 B1 teaches an AGC control.

Tsurumi et al U.S. Patent No 6,498,929 B1 teaches a receiver having DC offset.

Weiland et al U.S. Patent No 5,655,220 teaches a reverse link transmit power.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

1/6/06

EMMANUEL BAYARD
PRIMARY EXAMINER